REMARKS

A total of 23 claims remain in the present application.

Referring to the text of the Final Office Action:

- claims 1, 5, 6 and 17 stand rejected under 35 U.S.C. § 102(e), as being unpatentable over the teaching of United States Patent Application Publication No. 2003/0002779 (Bobin);

- claim 2 stands rejected under 35 U.S.C. § 103(a), as being unpatentable over the teaching of United States Patent Application Publication No. 2003/0002779 (Bobin) in view of United States Patent No. 6,822,975 (Antiosik);

- claims 4, 16 and 23 stand rejected under 35 U.S.C. § 103(a), as being unpatentable over the teaching of United States Patent Application Publication No. 2003/0002779 (Bobin) in view of United States Patent Application Publication No. 2003/0189925 (Wellbaum);

- claims 7-9 stand rejected under 35 U.S.C. § 103(a), as being unpatentable over the teaching of United States Patent Application Publication No. 2003/0002779 (Bobin) in view of United States Patent No. 6,411,631 (Sugawara);

- claims 10-12, 15, 18-20 and 24 stand rejected under 35 U.S.C. § 103(a), as being unpatentable over the teaching of United States Patent Application Publication No. 2003/0002779 (Bobin) in view of United States Patent Application Publication No. 2002/0126712 (Mueller) and further in view of United States Patent Application Publication No. 2003/0189925 (Wellbaum);

- claims 13 and 21 stand rejected under 35 U.S.C. § 103(a), as being unpatentable over the teaching of United States Patent Application Publication No. 2003/0002779 (Bobin) in view of United States Patent Application Publication No. 2002/0126712 (Mueller); and

- claims 14 and 22 stand rejected under 35 U.S.C. § 103(a), as being unpatentable over the teaching of United States Patent Application Publication

No. 2003/0002779 (Bobin) in view of United States Patent Application Publication No. 2002/0126712 (Mueller) and further in view of United States Patent No. 6,822,975 (Antiosik).

The Examiners above-noted claim rejections are believed to be traversed in view of the following discussion.

At page 3 of the detailed action, the Examiner asserts:

> "Bobin discloses that switching circuits can be configured independently (Independent pointer processing)(pg.4, para 67, lines 1-2). Bobin shows in FIG. 4 10Gbit/second signal 401 that feeds into a slicer 402, which divides input signal 401 into four 2.5 Gbit/second signals/slices (STS concatenation) that feed into switching circuits 404-407 (pg. 3, para. 50, lines 4-7). Bobin further discloses that if there is a small skew in path delay across the four lanes as they are received at the splicer, a special circuitry synchronizes traffic on the four lanes to eliminate the skew (successful pointer processing) by queuing and inserting special "synchronization characters" (pg. 3, para. 60, lines 1-9; claim – modifying at least one sub-stream to emulate a conventional STS concatenation with sufficient accuracy to enable successful pointer processing through the shelf)."

With respect, the person of ordinary skill in the art will instantly recognise that none or these assertions, particularly as they relate to the very well known SONET standard, are supported by the teaching of Bobin. More particularly, and taking each statement in turn:

Bobin does disclose that switching circuits 404-407 can be configured independently, but this does not teach or suggest the independent pointer processing required by claims 1 and 17. In fact, Bobin teaches directly away from the claimed invention, by teaching that the switching circuits may be "implemented as cross-bar switches" (Para. 38, lines 4-6). The person of ordinary skill in the art will immediately recall that a cross-bar switch does not perform pointer processing, and does not contain (or use) a pointer processing state machine much less the independent pointer processing state machines required by claims 1 and 17. While it is possible to speculate that other types of

non-blocking switches may be used, the fact that a cross-bar switch is acceptable means that Bobin is expressly teaching away from systems in which pointer processing is required.

In that respect, it should be noted that the term "pointer processing" is very well known in the art as relating processing functions performed on the pointers of an STS frame header and the SPE. See, for example, the SONET Telecommunications Standard Primer, Tektronix, http://www.tek.com/Measurement/App_Notes/SONET/2RW_11407_2.pdf. As is also very well known in the art, a cross-bar switch merely provides a propagation path between an input port and an output port, and does not provide any signal processing (much less pointer processing) functionality.

Bobin shows in FIG. 4 10Gbit/second signal 401 that feeds into a slicer 402, which divides input signal 401 into four 2.5 Gbit/second substreams that are supplied to respective switching circuits 404-407. The person of ordinary skill in the art will recognise that the slicing function of Bobin can be performed in any of a wide variety of ways, and Bobin does not provide any guidance as to which of these might be preferable. More particularly, Bobin does not teach or suggest that the 10Gbit/second signal 401 at STS frame boundaries, which would be necessary in order for the substreams to emulate an STS concatenation. While it is possible to speculate that the slicer 402 of Bobin could divide the 10Gbit/second signal 401 in this manner, the fact remains that Bobin provides no such teaching. Further, since each 2.5 Gbit/second substream is routed through a cross-bar switch circuit, there is no motivation for doing so.

Bobin discloses that if there is a small skew in path delay across the four lanes as they are received at the splicer, a special circuitry synchronizes traffic on the four lanes to eliminate the skew. The Examiner's application of this teaching to "successful pointer processing" is not understood. More particularly, it is not understood what the Examiner means by the term "successful pointer processing", or how this is intended to relate to skew in path delay.

The person of ordinary skill in the art will recognise that the "skew" referred to by Bobin relates entirely to the different delays incurred by each of the substreams as they traverse their respective switch circuits between the slicer 402 and the splicer 408. These different delays produce a skew between the subsignals arriving at the splicer 408. As is well known in the art, pointer processing involves manipulation of STS frame pointers and

the SPE. Thus for example, pointer processing of an STS signal will frequently result in the insertion of stuffs and/or a shift in the starting location of the SPE within the STS frame. Neither of these changes are related to path delays, and neither will be altered by any method used to compensate skew in path delay, including the methods alluded to by Bobin. However, prior to the teaching of the present invention, both of these changes would preclude successful recombination of independently pointer processed substreams into a single outgoing signal.

Furthermore, the person of ordinary skill in the art will recognise that "queuing and inserting special 'synchronization characters' " does not teach or suggest "modifying at least one sub-stream to emulate a conventional Synchronous Transport System (STS) concatenation ... " as required by claims 1 and 17. Rather, the ordinarily skilled artisan will recognise that Bobin is referring to a well known method of signal alignment, in which a synchronization character (usually a predetermined sequence of bits) is inserted into each substream at the point of origin (in this case the slicer 402 – see para 60, lines 8-10) Detection of the synchronization character in each substream at the splicer 408 enables the substreams to be realigned. However, the skilled artisan will recognise that the mere insertion of 'synchronization characters' at the slicer 402, as provided by Bobin, cannot possibly yield a substream which emulates a conventional STS concatenation, as required by claims 1 and 17.

In light of the foregoing, it is respectfully submitted that the presently claimed invention is clearly distinguishable over the teaching of United States Patent Application Publication No. 2003/0002779 (Bobin). None of the other cited references provide the missing teaching. More particularly, none of the known prior art teach or suggest "modifying at least one sub-stream to emulate a conventional Synchronous Transport System (STS) concatenation with sufficient accuracy to enable successful pointer processing through a shelf", as required by the presently-claimed invention.

In light of the foregoing, it is respectfully submitted that the presently claimed invention is clearly distinguishable over the teaching of the cited references, taken alone or in any combination. Thus it is believed that the present application is in condition for allowance, and early action in that respect is courteously solicited.

AMENDMENT UNDER 37 CFR § 1.116
Serial No. 09/992,410

If any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this response, such extension is hereby respectfully requested. If there are any fees due under 37 C.F.R. §§ 1.16 or 1.17 which are not enclosed herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 19-5113.

Respectfully submitted,

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